	L #	Hits	Search Text	DBs
1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin$3 near50 1	USPAT; US-PGPUB
3	L3	777	(exception fault trap$4) near20 1	USPAT; US-PGPUB
4	L4	12071	insert$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB
14	L16	192	(floating adj point) near50 pipelin$3	EPO; JPO; DERWENT; IBM_TDB
15	L17	108	(floating adj point) near20 (exception trap$4 fault)	EPO; JPO; DERWENT; IBM_TDB
16	L18	60	(insert$3 near10 (instruction command)) near50 (exception trap$4 fault)	EPO; JPO; DERWENT; IBM_TDB
17	L19	125953	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3 singl$3) near50 (state status)	EPO; JPO; DERWENT; IBM_TDB
18	L21	22	16 and 17	EPO; JPO; DERWENT; IBM_TDB
19	L20	4	(16 17) and (18 19)	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20030126419 A1	☐	Exception masking in binary translation	712/244
2	US 20020032718 A1	☐	METHOD AND APPARATUS FOR MAINTAINING TRANSLATED ROUTINE STACK IN A BINARY TRANSLATION ENVIROMENT	709/107
3	US 6549959 B1	☐	Detecting modification to computer memory by a DMA device	710/22
4	US 6535903 B2	☐	Method and apparatus for maintaining translated routine stack in a binary translation environment	709/100
5	US 6502237 B1	☐	Method and apparatus for performing binary translation method and apparatus for performing binary translation	717/136
6	US 6397379 B1	☐	Recording in a program execution profile references to a memory-mapped active device	717/140
7	US 6226789 B1	☐	Method and apparatus for data flow analysis	717/138
8	US 6199095 B1	☐	System and method for achieving object method transparency in a multi-code execution environment	709/107
9	US 6134573 A	☐	Apparatus and method for absolute floating point register addressing	708/510
10	US 5918097 A	☐	Fast translation and execution of a computer program on a non-native architecture by use of background translator	717/138
11	US 6000028 A	☐	Means and apparatus for maintaining condition codes in an unevaluated state	712/226
12	US 5930509 A	☐	Method and apparatus for performing binary translation	717/159
13	US 5915117 A	☐	Computer architecture for the deferral of exceptions on speculative instructions	710/262
14	US 5842017 A	☐	Method and apparatus for forming a translation unit	717/158
15	US 5835967 A	☐	Adjusting prefetch size based on source of prefetch address	711/213
16	US 5835951 A	☐	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
17	US 5802373 A	☐	Method for providing a pipeline interpreter for a variable length instruction set	717/139
18	US 5778211 A	☐	Emulating a delayed exception on a digital computer having a corresponding precise exception mechanism	703/26
19	US 5740416 A	☐	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
20	US 5732253 A	☐	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
21	US 5732243 A	☐	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
22	US 5706491 A	☐	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234

	Document ID	U	Title	Current OR
23	US 5692168 A	☐	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
24	US 5652900 A	☐	Data processor having 2n bits width data bus for context switching function	709/100
25	US 5560036 A	☐	Data processing having incircuit emulation function	712/227
26	US 5548736 A	☐	Method and apparatus overcoming delay introduced by instruction interlocking in pipelined instruction execution	712/244
27	US 5502827 A	☐	Pipelined data processor for floating point and integer operation with exception handling	712/244
28	US 5481734 A	☐	Data processor having 2n bits width data bus for context switching function	712/225
29	US 5440757 A	☐	Data processor having multistage store buffer for processing exceptions	712/228

	Document ID	U	Title	Current OR
1	US 20020 17432 3 A1	☐	Floating point unit pipeline synchronized with processor pipeline	712/220
2	US 64185 28 B1	☒	Floating point unit pipeline synchronized with processor pipeline	712/212
3	US 59699 75 A	☒	Data processing apparatus registers	708/490
4	US 58812 63 A	☒	Non-instruction base register addressing in a data processing apparatus	712/217
5	US 58812 59 A	☒	Input operand size and hi/low word selection control in data processing systems	712/210
6	US 58812 57 A	☒	Data processing system register control	712/200
7	US 58600 00 A	☒	Floating point unit pipeline synchronized with processor pipeline	712/244
8	US 58124 39 A	☒	Technique of incorporating floating point information into processor instructions	708/497
9	US 57846 02 A	☒	Method and apparatus for digital signal processing for integrated circuit architecture	712/220
10	US 56665 37 A	☒	Power down scheme for idle processor components	713/322
11	US 56492 08 A	☒	Mechanism for handling non-maskable interrupt requests received from different sources	710/262
12	US 56383 06 A	☒	Testing hooks for testing an integrated data processing system	702/119
13	US 56301 53 A	☒	Integrated digital signal processor/general purpose CPU with shared internal memory	712/35
14	US 56258 28 A	☒	Parallel operating CPU core and DSP module for executing sequence of vector DSP code instructions to generate decoded constellation points in QAM/TCM modem application	375/261
15	US 56131 49 A	☒	Integrated data processing system utilizing successive approximation analog to digital conversion and PWM for parallel disconnect	712/36
16	US 56067 14 A	☒	Integrated data processing system including CPU core and parallel, independently operating DSP module and having multiple operating modes	712/43
17	US 56030 17 A	☒	Parallel integrated circuit having DSP module and CPU core operable for switching between two independent asynchronous clock sources while the system continues executing instructions	713/501
18	US 55926 77 A	☒	Integrated data processing system including CPU core and parallel, independently operating DSP module	712/34
19	US 55903 57 A	☒	Integrated CPU core and parallel, independently operating DSP module and time-critical core priority scheme	712/35
20	US 55902 94 A	☒	Method and apparatus for retarting pipeline processing	712/244
21	US 55375 38 A	☒	Debug mode for a superscalar RISC processor	714/38
22	US 55308 15 A	☒	Apparatus and method for verifying the order and operation of a data processing device when asynchronous commands are held in a command queue	712/227

	Document ID	U	Title	Current R
23	US 5519879 A	☒	Integrated circuit having CPU and DSP for executing vector lattice propagation instruction and updating values of vector Z in a single instruction cycle	712/35
24	US 5491828 A	☒	Integrated data processing system having CPU core and parallel independently operating DSP module utilizing successive approximation analog to digital and PWM for parallel disconnect	712/35
25	US 5487173 A	☒	DTMF detection in an integrated data processing system	712/35
26	US 5301331 A	☒	Interruption handling system	710/260
27	US 4879676 A	☐	Method and apparatus for precise floating point exceptions	708/505

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1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin$3 near50 1	USPAT; US-PGPUB
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4	L4	12071	insert$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB
14	L16	192	(floating adj point) near50 pipelin$3	EPO; JPO; DERWENT; IBM_TDB
15	L17	108	(floating adj point) near20 (exception trap$4 fault)	EPO; JPO; DERWENT; IBM_TDB
16	L18	60	(insert$3 near10 (instruction command)) near50 (exception trap$4 fault)	EPO; JPO; DERWENT; IBM_TDB
17	L19	125953	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3 singl$3) near50 (state status)	EPO; JPO; DERWENT; IBM_TDB
18	L21	22	16 and 17	EPO; JPO; DERWENT; IBM_TDB
19	L20	4	(16 17) and (18 19)	EPO; JPO; DERWENT; IBM_TDB
20	L22	0	(2 3) and (6 7) and 9 not (10 12 15)	USPAT; US-PGPUB
21	L24	0	9 and (precise$3 and exception).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
22	L23	11	9 and (precise$3 and exception).ab,ti.	USPAT; US-PGPUB
23	L25	537	(translat$3 target) near50 1	USPAT; US-PGPUB
24	L27	29	3 near99 25	USPAT; US-PGPUB
25	L28	27	(exception fault trap$4) near10 precise$3 near99 2	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20020 17432 3 A1	☐	Floating point unit pipeline synchronized with processor pipeline	712/220
2	US 64185 28 B1	☒	Floating point unit pipeline synchronized with processor pipeline	712/212
3	US 60214 88 A	☒	Data processing system having an apparatus for tracking a status of an out-of-order operation and method thereof	712/228
4	US 59665 30 A	☒	Structure and method for instruction boundary machine state restoration	712/244
5	US 58600 00 A	☒	Floating point unit pipeline synchronized with processor pipeline	712/244
6	US 58124 39 A	☒	Technique of incorporating floating point information into processor instructions	708/497
7	US 56734 26 A	☒	Processor structure and method for tracking floating-point exceptions	712/244
8	US 56491 36 A	☒	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
9	US 55465 54 A	☒	Apparatus for dynamic register management in a floating point unit	711/203
10	US 55375 38 A	☒	Debug mode for a superscalar RISC processor	714/38
11	US 48796 76 A	☐	Method and apparatus for precise floating point exceptions	708/505

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1	L1	13583	floating adj point	USPAT; US-PGPUB
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4	L4	12071	insert$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB
14	L16	192	(floating adj point) near50 pipelin$3	EPO; JPO; DERWENT; IBM_TDB
15	L17	108	(floating adj point) near20 (exception trap$4 fault)	EPO; JPO; DERWENT; IBM_TDB
16	L18	60	(insert$3 near10 (instruction command)) near50 (exception trap$4 fault)	EPO; JPO; DERWENT; IBM_TDB
17	L19	125953	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3 singl$3) near50 (state status)	EPO; JPO; DERWENT; IBM_TDB
18	L21	22	16 and 17	EPO; JPO; DERWENT; IBM_TDB
19	L20	4	(16 17) and (18 19)	EPO; JPO; DERWENT; IBM_TDB
20	L22	0	(2 3) and (6 7) and 9 not (10 12 15)	USPAT; US-PGPUB
21	L24	0	9 and (precise$3 and exception).ab,ti.	EPO; JPO; DERWENT; IBM_TDB
22	L23	11	9 and (precise$3 and exception).ab,ti.	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030 08435 3 A1	☐	System and method for predictive power ramping	713/300
2	US 20020 01690 3 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
3	US 65780 59 B1	☒	Methods and apparatus for controlling exponent range in floating-point calculations	708/496
4	US 64906 07 B1	☒	Shared FP and SIMD 3D multiplier	708/620
5	US 63706 39 B1	☒	Processor architecture having two or more floating-point status fields	712/222
6	US 63321 86 B1	☒	Vector register addressing	711/217
7	US 62826 34 B1	☒	Apparatus and method for processing data having a mixed vector/scalar register file	712/210
8	US 62826 30 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
9	US 62232 78 B1	☒	Method and apparatus for floating point (FP) status word handling in an out-of-order (000) Processor Pipeline	712/227
10	US 62125 39 B1	☒	Methods and apparatus for handling and storing bi-endian words in a floating-point processor	708/495
11	US 61890 94 B1	☒	Recirculating register file	712/222
12	US 61516 69 A	☒	Methods and apparatus for efficient control of floating-point status register	712/222
13	US 61450 49 A	☒	Method and apparatus for providing fast switching between floating point and multimedia instructions using any combination of a first register file set and a second register file set	710/267
14	US 60761 55 A	☒	Shared register architecture for a dual-instruction-set CPU to facilitate data exchange between the instruction sets	712/225
15	US 60493 43 A	☒	Graphics processing unit and graphics processing system	345/501
16	US 60386 53 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
17	US 59665 30 A	☒	Structure and method for instruction boundary machine state restoration	712/244
18	US 58840 62 A	☒	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	712/218
19	US 58570 89 A	☒	Floating point stack and exchange instruction	712/222
20	US 58322 92 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
21	US 58225 79 A	☒	Microprocessor with dynamically controllable microcontroller condition selection	712/245
22	US 58093 20 A	☒	High-performance multi-processor having floating point unit	712/34

	Document ID	U	Title	Current OR
23	US 5805918 A	☒	Dual-instruction-set CPU having shared register for storing data before switching to the alternate instruction set	712/43
24	US 5781790 A	☒	Method and apparatus for performing floating point to integer transfers and vice versa	712/23
25	US 5696955 A	☒	Floating point stack and exchange instruction	712/222
26	US 5685009 A	☒	Shared floating-point registers and register port-pairing in a dual-architecture CPU	712/23
27	US 5673426 A	☒	Processor structure and method for tracking floating-point exceptions	712/244
28	US 5668984 A	☒	Variable stage load path and method of operation	712/222
29	US 5649136 A	☒	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
30	US 5606696 A	☒	Exception handling method and apparatus for a microkernel data processing system	709/108
31	US 5583805 A	☒	Floating-point processor having post-writeback spill stage	708/495
32	US 5560032 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
33	US 5546554 A	☒	Apparatus for dynamic register management in a floating point unit	711/203
34	US 5537538 A	☒	Debug mode for a superscalar RISC processor	714/38
35	US 5504925 A	☒	Apparatus and method for implementing interrupts in pipelined processors	712/244
36	US 5502827 A	☒	Pipelined data processor for floating point and integer operation with exception handling	712/244
37	US 5481719 A	☒	Exception handling method and apparatus for a microkernel data processing system	709/108
38	US 5481693 A	☒	Shared register architecture for a dual-instruction-set CPU	712/225
39	US 5420989 A	☒	Coprocessor interface supporting I/O or memory mapped communications	710/110
40	US 5418916 A	☒	Central processing unit checkpoint retry for store-in and store-through cache systems	712/228
41	US 5155843 A	☒	Error transition mode for multi-processor system	714/5
42	US 5153848 A	☒	Floating point processor with internal free-running clock	708/503
43	US 5051885 A	☒	Data processing system for concurrent dispatch of instructions to multiple functional units	712/215
44	US 5042000 A	☒	Integral transform method	708/404
45	US 4879676 A	☒	Method and apparatus for precise floating point exceptions	708/505

	Document ID	U	Title	Current OR
46	US 4805128 A	☒	Format conversion system	708/204
47	US 4763294 A	☒	Method and apparatus for floating point operations	708/510
48	US 4736291 A	☒	General-purpose array processor	712/11
49	US 3872442 A	☐	SYSTEM FOR CONVERSION BETWEEN CODED BYTE AND FLOATING POINT FORMAT	708/204

	Document ID	U	Title	Current OR
1	US 20030135722 A1	☐	Speculative load instructions with retry	712/235
2	US 20030061470 A1	☒	Power consumption reduction mechanism for pipeline stalls	712/219
3	US 20030061467 A1	☒	Scoreboarding mechanism in a pipeline that includes replays and redirects	712/217
4	US 20030061465 A1	☒	Issue and retirement mechanism in processor having different pipeline lenghths	712/214
5	US 20030009648 A1	☒	Apparatus for supporting a logically partitioned computer system	711/202
6	US 6499123 B1	☒	Method and apparatus for debugging an integrated circuit	714/724
7	US 6438671 B1	☒	Generating partition corresponding real address in partitioned mode supporting system	711/173
8	US 6311261 B1	☒	Apparatus and method for improving superscalar processors	712/23
9	US 6304963 B1	☒	Handling exceptions occuring during processing of vector instructions	712/244
10	US 6247113 B1	☒	Coprocessor opcode division by data type	712/200
11	US 6240508 B1	☒	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
12	US 6212629 B1	☒	Method and apparatus for executing string instructions	712/241
13	US 6205560 B1	☒	Debug system allowing programmable selection of alternate debug mechanisms such as debug handler, SMI, or JTAG	714/34
14	US 6170001 B1	☒	System for transfering format data from format register to memory wherein format data indicating the distribution of single or double precision data type in the register bank	708/495
15	US 6138230 A	☒	Processor with multiple execution pipelines using pipe stage state information to control independent movement of instructions between pipe stages of an execution pipeline	712/216
16	US 6112019 A	☒	Distributed instruction queue	712/214
17	US 6073231 A	☒	Pipelined processor with microcontrol of register translation hardware	712/218
18	US 6021486 A	☒	Continued processing of out-of-order non-architectual operations upon exceptions until flushing by architectual operations exceptions to avoid resume deadlock	712/218
19	US 5838897 A	☒	Debugging a processor using data output during idle bus cycles	714/30
20	US 5835967 A	☒	Adjusting prefetch size based on source of prefetch address	711/213
21	US 5835951 A	☒	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145

	Document ID	U	Title	Current OR
22	US 5809552 A	☒	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
23	US 5784636 A	☒	Reconfigurable computer architecture for use in signal processing applications	712/37
24	US 5784589 A	☒	Distributed free register tracking for register renaming using an availability tracking register associated with each stage of an execution pipeline	712/217
25	US 5781753 A	☒	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
26	US 5768575 A	☒	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
27	US 5764938 A	☒	Resynchronization of a superscalar processor	712/200
28	US 5758112 A	☒	Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction	712/217
29	US 5751985 A	☒	Processor structure and method for tracking instruction status to maintain precise state	712/218
30	US 5740416 A	☒	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
31	US 5732253 A	☒	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
32	US 5732243 A	☒	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
33	US 5706491 A	☒	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
34	US 5692168 A	☒	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
35	US 5673408 A	☒	Processor structure and method for renamable trap-stack	712/216
36	US 5659721 A	☒	Processor structure and method for checkpointing instructions to maintain precise state	712/228
37	US 5655115 A	☒	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
38	US 5651124 A	☒	Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state	712/215
39	US 5649225 A	☒	Resynchronization of a superscalar processor	712/23
40	US 5644742 A	☒	Processor structure and method for a time-out checkpoint	712/244
41	US 5630149 A	☒	Pipelined processor with register renaming hardware to accommodate multiple size registers	712/217
42	US 5611071 A	☒	Split replacement cycles for sectored cache lines in a 64-bit microprocessor interfaced to a 32-bit bus architecture	711/133

	Document ID	U	Title	Current OR
43	US 5596733 A	☒	System for exception recovery using a conditional substitution instruction which inserts a replacement result in the destination of the excepting instruction	712/244
44	US 5596731 A	☒	Single clock bus transfers during burst and non-burst cycles	710/305
45	US 5590359 A	☒	Method and apparatus for generating a status word in a pipelined processor	712/32
46	US 5590294 A	☒	Method and apparatus for retarting pipeline processing	712/244
47	US 5560036 A	☒	Data processing having incircuit emulation function	712/227
48	US 5546551 A	☒	Method and circuitry for saving and restoring status information in a pipelined computer	707/102
49	US 5544342 A	☒	System and method for prefetching information in a processing system	711/119
50	US 5542058 A	☒	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
51	US 5488730 A	☒	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
52	US 5481689 A	☒	Conversion of internal processor register commands to I/O space addresses	711/202
53	US 5471591 A	☒	Combined write-operand queue and read-after-write dependency scoreboard	712/217
54	US 5450555 A	☒	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
55	US 5394529 A	☒	Branch prediction unit for high-performance processor	712/240
56	US 5333296 A	☒	Combined queue for invalidates and return data in multiprocessor system	711/171
57	US 5317720 A	☐	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143

	Document ID	U	Title	Current OR
1	US 20030126419 A1	☐	Exception masking in binary translation	712/244
2	US 6480818 B1	☒	Debugging techniques in a multithreaded environment	703/26
3	US 6295601 B1	☒	System and method using partial trap barrier instruction to provide trap barrier class-based selective stall of instruction processing pipeline	712/244
4	US 6115811 A	☒	Digital data process system including efficient arrangement to support branching within trap shadows	712/244
5	US 6009515 A	☒	Digital data processing system including efficient arrangement to support branching within trap shadows	712/244
6	US 5961630 A	☒	Method and apparatus for handling dynamic structural hazards and exceptions by using post-ready latency	712/200
7	US 5887160 A	☒	Method and apparatus for communicating integer and floating point data over a shared data path in a single instruction pipeline processor	712/222
8	US 5809271 A	☒	Method and apparatus for changing flow of control in a processor	712/208
9	US 5729728 A	☒	Method and apparatus for predicting, clearing and redirecting unpredicted changes in instruction flow in a microprocessor	712/234
10	US 5687338 A	☒	Method and apparatus for maintaining a macro instruction for refetching in a pipelined processor	712/205
11	US 5301312 A	☐	Method and system for utilizing benign fault occurrence to measure interrupt-blocking times	714/32

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1	L1	13583	floating adj point	USPAT; US-PGPUB
2	L2	1105	pipelin$3 near50 1	USPAT; US-PGPUB
3	L3	777	(exception fault trap$4) near20 1	USPAT; US-PGPUB
4	L4	12071	insert$3 near10 (command instruction)	USPAT; US-PGPUB
5	L5	3	3 near99 4	USPAT; US-PGPUB
6	L6	142	(exception fault trap$4) near50 4	USPAT; US-PGPUB
7	L7	129670	(return$3 roll$3 unroll$3 play$3 replay$3 (re adj execut$3) reexecut$3) near50 (state status)	USPAT; US-PGPUB
8	L8	438	(2 3 6) and 7	USPAT; US-PGPUB
9	L9	19000	floating.ab,ti.	USPAT; US-PGPUB
10	L11	278	2 and 3 not 10	USPAT; US-PGPUB
11	L10	49	8 and 9	USPAT; US-PGPUB
12	L12	57	8 and 11 not 10	USPAT; US-PGPUB
13	L15	11	3 and 6 not (10 12)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 05233 229 A	☐	INFORMATION PROCESSOR AND INFORMATION PROCESSING METHOD	
2	JP 02010 427 A	☒	METHOD AND DEVICE FOR PRECISE FLOATING POINT EXCEPTION	
3	EP 77957 7 A2	☒	Micoprocessor pipe control and register translation	
4	EP 68455 2 A1	☒	PROCESSOR SYSTEM AND DEBUG MODE ACCOMPLISHMENT METHOD.	
5	EP 64908 6 A1	☒	Microprocessor with speculative execution.	
6	EP 64908 5 A1	☒	Microprocessor pipe control and register translation.	
7	EP 30689 1 A2	☒	Pipelined slave protocol for high performance CPU-FPU cluster.	
8	NB940 6211	☒	Interface to a Floating Point Processor	
9	NN911 117	☒	Efficient Operating System Support for Floating Point Trapping on a Heavily Pipelined Hardware Architecture.	
10	US 62090 83 B	☒	Processor operating method for computer systems, involves delaying issue of next instruction until floating point unit clears preceding instruction, in normal operational mode	
11	JP 11327 903 A	☒	Operation execution controller of floating point unit in computer system - checks corresponding system register mark, when event requiring milli code emulation is detected dynamically, based on which completion or restriction of operation is judged	
12	US 58840 62 A	☒	Superscalar pipelined microprocessor integrated circuit in data processing system	
13	US 58840 57 A	☒	System for temporal realignment of floating point pipeline to integer pipeline for emulation of load operate architecture on load/store processor	
14	US 57297 29 A	☒	Fast trap ordering for pipelined multiscalar microprocessor - includes early and late trap units in execution units with mask generation logic coupling trap units to registers	
15	US 55599 77 A	☒	Floating point instruction pair in pipelined processor - involves stalling following floating point instruction in execution stage if immediate floating point instruction pair is capable of raising exception	
16	US 55028 27 A	☒	Pipelined data processor for floating point and integer operation with exception handling - has control unit which, when exception signal is asserted by execution unit, writes new data to register, receives exception, and activates exception processing handler	
17	EP 68455 2 B	☒	Processor system with debug mode accomplishment method - has interrupt unit switching between normal and debug modes where command not executed until judged whether exception produced	
18	US 54169 12 A	☒	Pipeline parallel processing units executions exception handling - receiving first floating point instruction from control memory and storing it in first and second latching devices	
19	EP 64908 6 A	☒	Pipelined microprocessor with speculative instruction execution - issues speculation instructions e.g branches and floating point instructions and checks processor state to enable execution pipeline repair for branch mis-prediction or floating point exception	
20	US 53073 01 A	☒	Safe instruction recognition for pipelined floating-point processor - analyses exponents of each operand, which are declared safe to ensure against floating-point processor overflow and underflow exceptions for add, subtract, multiply and divide operations	

	Document ID	U	Title	Current OR
21	EP 588252 A	☒	Instruction processing appts. for pipelined processors - has floating point register with several addressable storage elements for operand data, two address receiver circuits, register output, instruction execution unit with exception circuit, and shift register	
22	EP 306891 A	☐	Pipelined slave protocol for high performance CPU-fpu cluster - uses storage on CPU for status information related to floating point co-processor and uses overlapped execution	

	Document ID	U	Title	Current OR
1	JP 2001147809 A	☐	COMPUTER SYSTEM AND METHOD FOR DECIDING EXISTENCE OF FPU IN COMPUTER SYSTEM	
2	EP 903664 A2	☒	Floating-point processor with operand-format precision greater than execution precision	
3	US 5961630 A	☒	Instruction scheduling method for execution in digital processor	
4	EP 287115 A	☐	Floating point arithmetic co-processor control system - divides functions of co-processor into separate streams for pipeline control and stores instructions in FIFO	